ABSTRACT OF THE DISCLOSURE

A shift information latch circuit includes a plurality of latch portions provided corresponding to memory cell rows, respectively, and a fuse circuit transmitting fuse data produced corresponding to an address of a faulty memory cell row. The plurality of latch portion successively receive fuse data, and each transmit a shift control signal instructing a shift operation. In response to this shift control signal, a row decoder and a match line amplifier execute a shift operation for repairing the faulty memory cell row. In this structure, a decoder circuit decoding the address of the faulty memory cell row is not arranged so that a whole area of the circuits executing the shift operation is reduced, and the shift operation can be easily executed.